8-bit universal shift/storage register with synchronous reset and common I/O pins (3-State)

74F323

FEATURES

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: Shift left, shift right, load, and store
- 3-State outputs for bus-oriented applications

DESCRIPTION

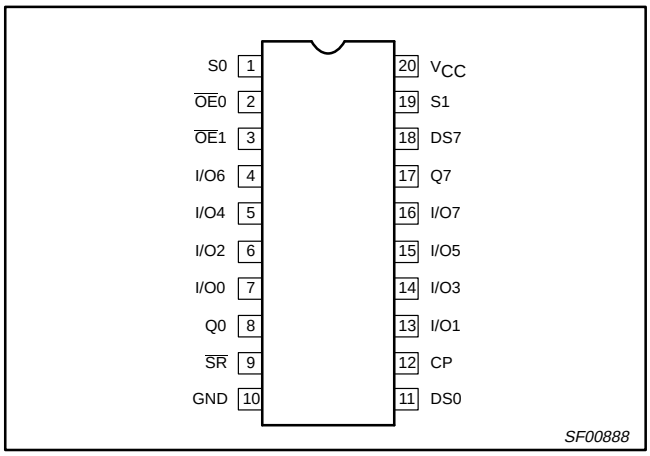
The 74F323 is an 8-bit universal shift/storage register with 3-State outputs. Its function is similar to the 74F299 with the exception of synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs and outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. Four modes of operation are possible: Hold (store), shift left, shift right, and parallel load.

The 74F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load, and hold operations. The type of operation is determined by S0 and S1, as shown in the Function Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{SR}$ overrides the Select and inputs and allows the flip-flops to be reset by the next rising edge of clock. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of clock are observed.

A High signal on either $\overline{OE}0$ or $\overline{OE}1$ disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S0 and S1 in preparation for a parallel load operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	115MHz	55mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20-pin plastic DIP	N74F323N
20-pin plastic SOL	N74F323D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

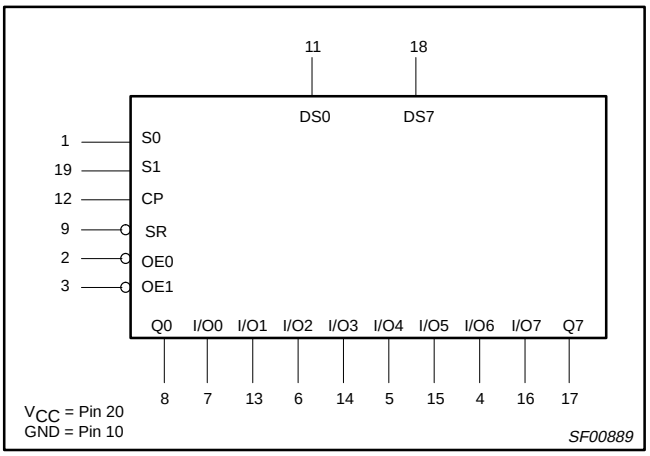
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S0, S1	Mode select inputs	1.0/2.0	20µA/1.2mA
CP	Clock pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (Active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}0$, $\overline{OE}1$	Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
Q0, Q7	Serial outputs	50/33	20µA/20mA
I/On	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-State parallel outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High State and 0.6mA in the Low state.

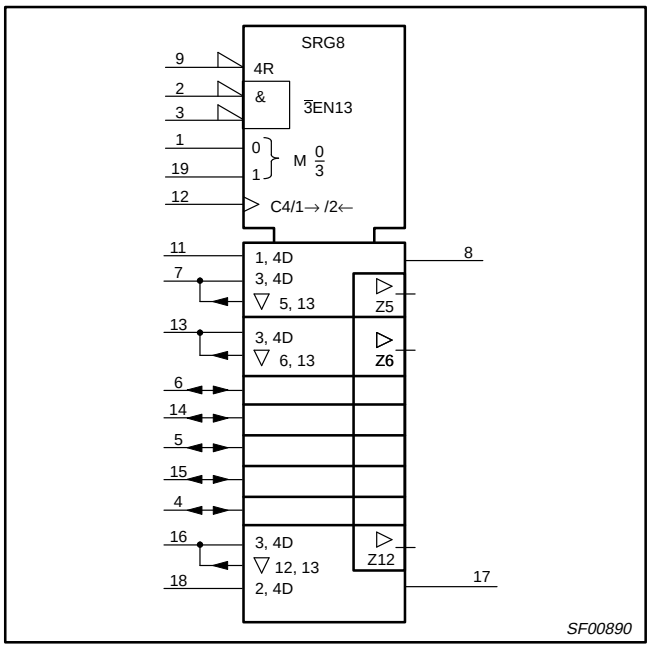
8-bit universal shift/storage register with synchronous reset and common I/O pins (3-State)

74F323

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

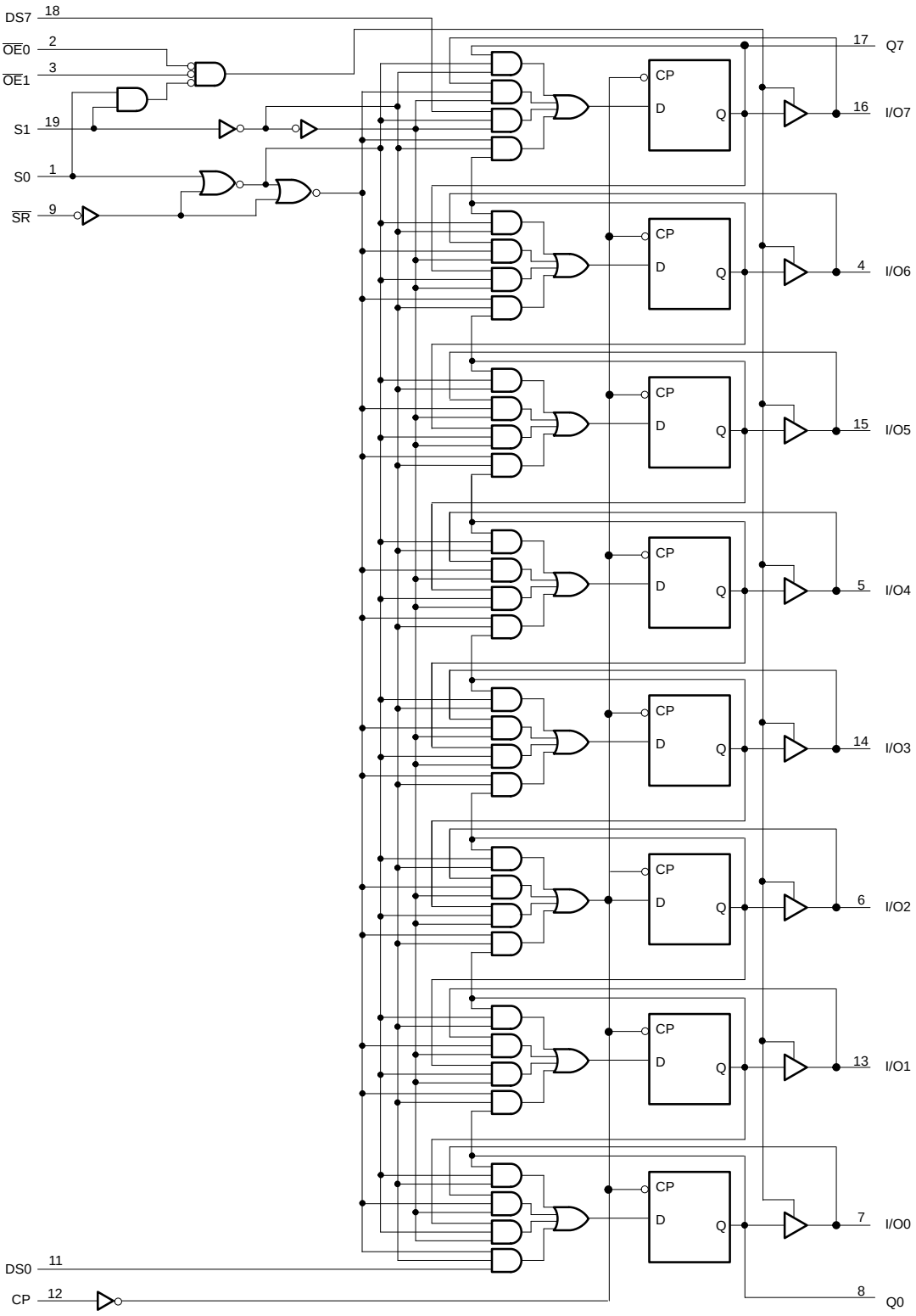


FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}$n	$\overline{SR}$	S1	S0	CP	
L	L	X	X	↑	Synchronous Reset; Q0 - Q7 = Low
L	H	H	H	↑	Parallel load; I/On → Qn
L	H	L	H	↑	Shift right; DS0 → Q0, Q0 → Q1, etc.
L	H	H	L	↑	Shift left; DS7 → Q7, Q7 → Q6, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs disabled (3-state)

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

SF00883

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q0, Q7	40	mA
		I/On	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	Q0, Q7			–1	mA
		I/On			–3	mA
I_{OL}	Low-level output current	Q0, Q7			20	mA
		I/On			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Q0, Q7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On		I_{OH} = –3mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/On	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	S0, S1	V_{CC} = MAX, V_I = 0.5V					–1.2	mA
		others						–0.6	mA
I_{IH} + I_{OZH}	Off-state output current, High-level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL} + I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	75	mA
		I_{CCL}					65	90	mA
		I_{CCZ}					55	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} =+ 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Qn		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q0 or Q7		Waveform 1	4.0 3.5	6.0 6.0	8.5 8.5	3.5 4.5	9.5 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to I/On		Waveform 1	4.0 5.0	6.0 6.5	9.0 9.5	4.0 4.0	10.0 10.0	ns ns
t_{PZH} t_{PZL}	Output Enable time Sn, $\overline{OE}$ to I/On		Waveform 3 Waveform 4	3.5 4.0	6.0 8.0	9.0 11.0	3.5 4.0	10.0 11.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time Sn, $\overline{OE}$ to I/On		Waveform 3 Waveform 4	2.5 1.5	5.0 3.0	7.5 5.5	2.5 1.5	8.0 6.5	ns ns

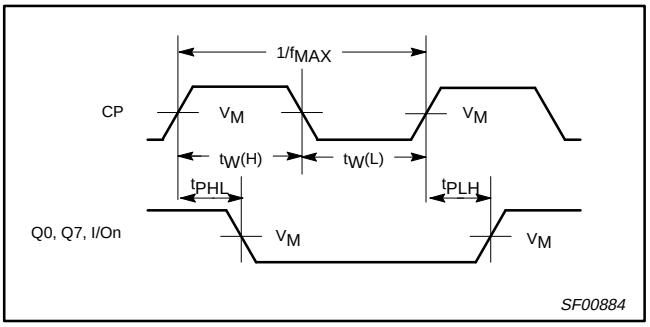
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low S0 or S1 to CP	Waveform 2	6.5 6.5			7.5 7.5		ns
t_h(H) t_h(L)	Hold time, High or Low S0 or S1 to CP	Waveform 2	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low I/O0, DS0 or DS7 to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low I/O0, DS0 or DS7 to CP	Waveform 2	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{SR}$ to CP	Waveform 2	7.0 7.0			8.5 8.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{SR}$ to CP	Waveform 2	0 0			0 0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	3.5 3.5			4.0 4.0		ns

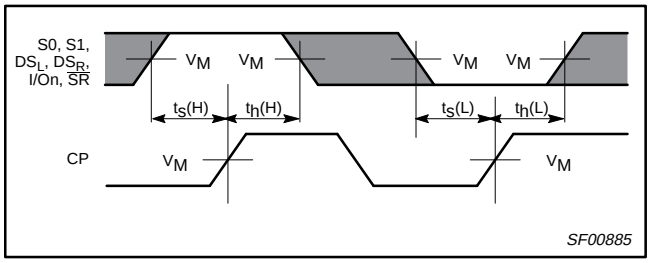
AC WAVEFORMS

For all waveforms, V_M = 1.5V

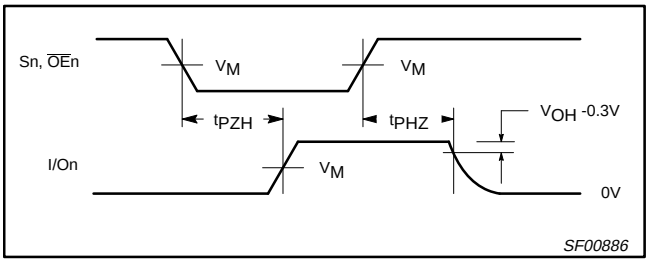
The shaded areas indicate when the input is permitted to change for predictable output performance.



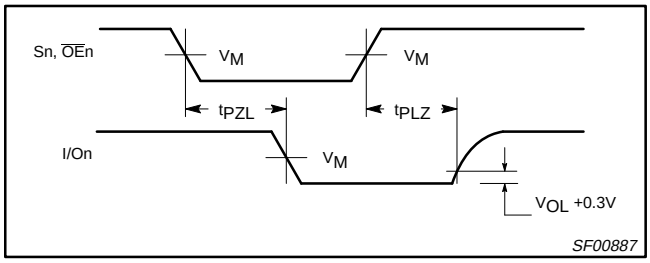
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data, Select and Reset Setup and Hold Times

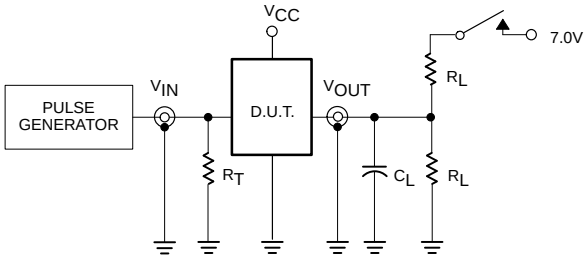


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

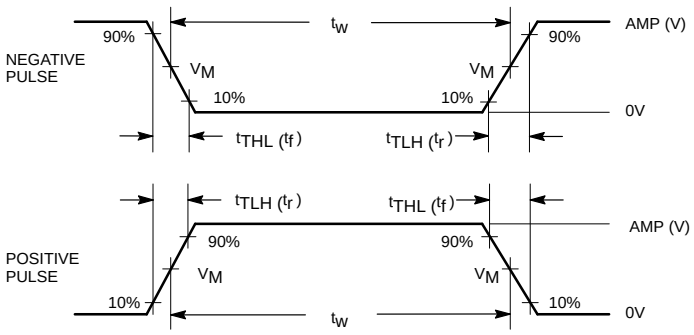


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777